AH125

½W High Linearity InGaP HBT Amplifier

Product Features

- 400 – 3600 MHz
- +28 dBm P1dB
- +45 dBm Output IP3
- 16.2 dB Gain @ 2140 MHz
- 150 mA current draw
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/Green/RoHS-compliant SOT-89 Package
- Class 2 HBM ESD rating (>2kV)

Applications

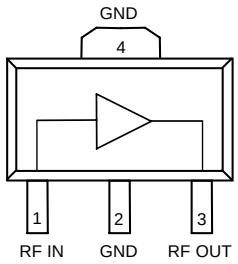
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA

Product Description

The AH125 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance across a broad range with +45 dBm OIP3 and +28 dBm of compressed 1dB power while drawing 150 mA current. The AH125 is available in a lead-free/green/RoHS-compliant SOT-89 package. All devices are 100% RF and DC tested.

The AH125 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. Internal biasing allows the AH125 to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations or repeaters.

Functional Diagram



Function	Pin No.
RF Input	1
RF Output / Vcc	3
Ground	2, 4

Specifications

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	400		3600
Test Frequency	MHz		2140	
Gain	dB	14	16.2	18
Input Return Loss	dB		12	
Output Return Loss	dB		12	
W-CDMA Channel Power[2] @ -50 dBc ACLR	dBm		+19	
Output P1dB	dBm		+28	
Output IP3[3]	dBm	+41	+45	
Noise Figure	dB		4.4	
Quiescent Collector Current	mA	130	150	170
Device Voltage	V		+5	

1. Test conditions unless otherwise noted: 25ºC, Vsupply = +5 V, in tuned application circuit.
2. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW
3. OIP3 is measured with two tones separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule. Measured at 17dBm/tone for 900 MHz, 14 dBm/tone for 1960 MHz, and 12 dBm/tone for 2140 MHz.

Typical Performance

Parameter	Units	Typical		
Frequency	MHz	920	1960	2140
Gain	dB	20	17	16.2
Input Return Loss	dB	20	16	12
Output Return Loss	dB	9.9	9	12
W-CDMA Channel Power[2] @ -50 dBc ACLR	dBm	+19	+19	+19
Output P1dB	dBm	+28.1	+27.8	+28.0
Output IP3 [3]	dBm	+47	+47	+45
Noise Figure	dB	7.7	4.6	4.4
Quiescent Collector Current	mA		150	
Device Voltage	V		+5	

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, CW, 50 Ω, T=25°C	Input P10dB
Device Voltage	+6 V
Max Junction Temperature, T_J For 10^6 hours MTTF	200 °C
Thermal Resistance, Θ_{JC}	64.3 °C / W

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

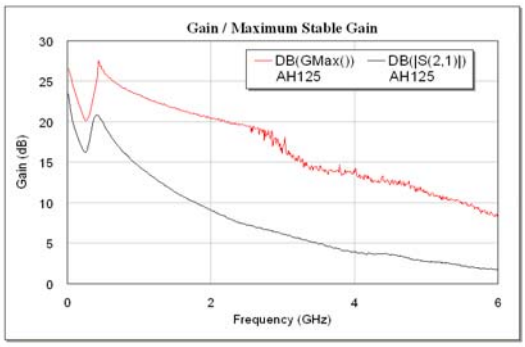
Part No.	Description
AH125-89G	½W High Linearity InGaP HBT Amplifier
AH125-89PCB900	900 MHz Evaluation Board
AH125-89PCB1960	1960 MHz Evaluation Board
AH125-89PCB2140	2140 MHz Evaluation Board
AH125-89PCB2600	2600 MHz Evaluation Board

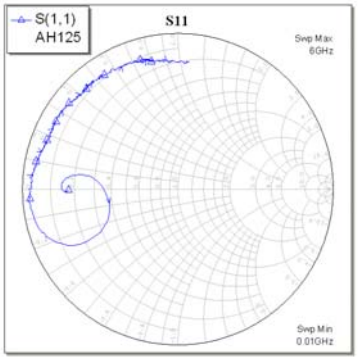
Standard T/R size = 1000 pieces on a 7" reel.

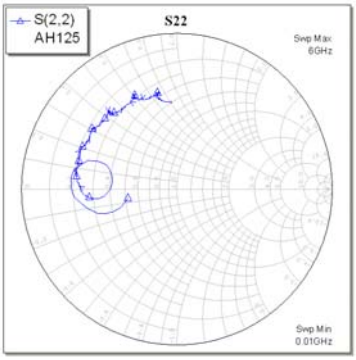
Specifications and information are subject to change without notice

Typical Device Data

S-Parameters (V_{Device} = +5 V, I_{CC} = 150 mA, 25 °C, unmatched 50 ohm system)







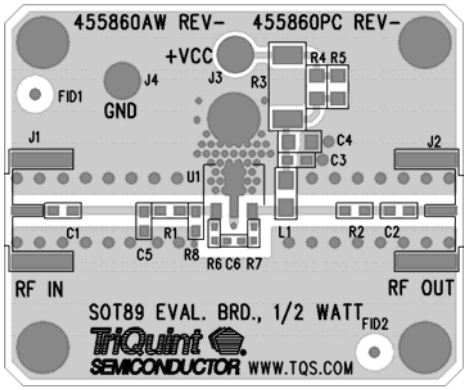
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line.

S-Parameters (V_{Device} = +5 V, I_{CC} = 150 mA, 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
100	-2.51	176.96	19.12	153.71	-33.85	-7.98	-4.58	-168.55
300	-6.65	-179.55	16.82	171.45	-41.51	-51.50	-3.50	167.66
500	-0.47	-166.72	19.86	129.11	-32.54	37.90	-6.46	-173.90
700	-0.50	179.58	16.95	110.14	-32.11	15.12	-4.57	-177.11
900	-0.56	173.91	15.09	99.64	-32.29	6.66	-4.14	177.58
1100	-0.65	170.52	13.68	91.32	-32.15	2.53	-3.89	173.40
1300	-0.78	166.87	12.37	83.49	-32.04	-2.50	-3.71	169.83
1500	-0.82	163.90	11.21	76.80	-32.11	-4.03	-3.64	167.10
1700	-0.93	161.34	10.11	71.12	-31.97	-7.89	-3.70	164.08
1900	-0.93	157.61	9.40	64.93	-31.94	-9.93	-3.64	160.19
2100	-0.94	154.21	8.47	58.83	-31.97	-10.87	-3.54	156.60
2300	-0.91	151.59	7.66	53.42	-31.80	-14.20	-3.48	153.92
2500	-0.93	149.24	7.06	49.26	-32.04	-16.18	-3.67	152.18
2700	-0.90	145.94	6.70	43.87	-31.63	-16.91	-3.72	147.67
2900	-0.96	143.87	6.12	39.45	-31.18	-18.50	-3.54	143.63
3100	-1.07	139.90	5.74	34.00	-31.37	-23.47	-3.52	141.32
3300	-1.18	136.50	5.09	29.36	-31.25	-20.88	-3.70	140.24
3500	-1.18	133.80	4.62	24.20	-31.12	-27.12	-3.72	135.07
3700	-1.11	132.39	4.12	20.26	-31.25	-26.33	-3.64	130.47

Device S-parameters are available for download off of the website at: http://www.tqs.com

Application Circuit PCB Layout



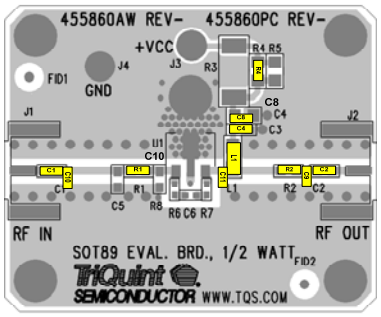
Circuit Board Material: .062" total thickness with a .014" FR4 top RF layer, 4 layers (other layers added for rigidity), 1 oz copper, ε_r = 4.3, Microstrip line details: width = .031", spacing = .035"

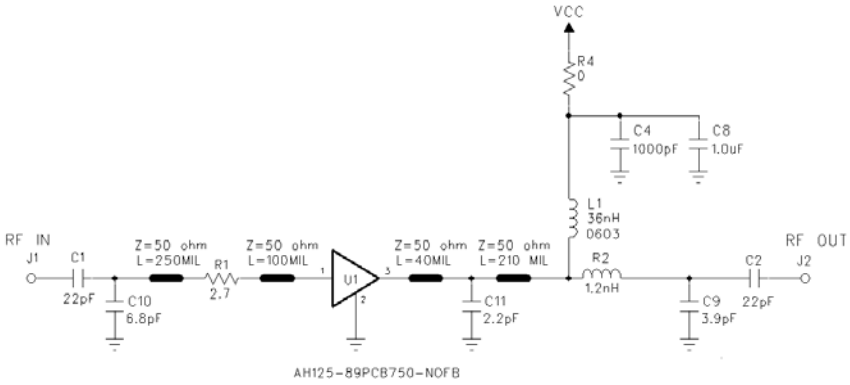
700-800 MHz Reference Design

802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW

Typical O-FDMA Performance at 25°C

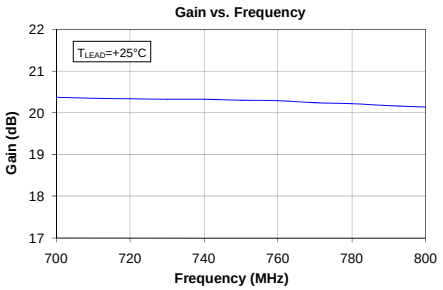
Frequency	700	750	800	MHz
Gain	20.4	20.3	20.1	dB
Input Return Loss	12	17	25	dB
Output Return Loss	7.5	6.8	6.3	dB
EVM Pout=+18 dBm	0.9	0.7	0.7	%
ACLR Pout=+18 dBm	-52.6	-56	-54.4	dBc
Output P1dB	+28.9	+29.4	+29.2	dBm
Output IP3 Pout=+18 dBm/tone, 1MHz spacing	+43.7	+46.2	+45.5	dBm
Quiescent Current, Icq	150			mA
Vcc	+5			V

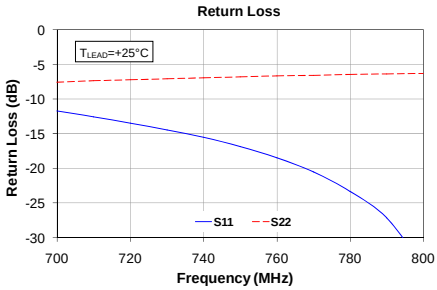


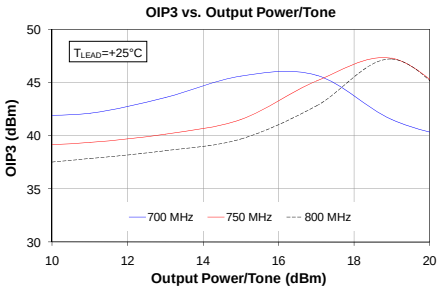


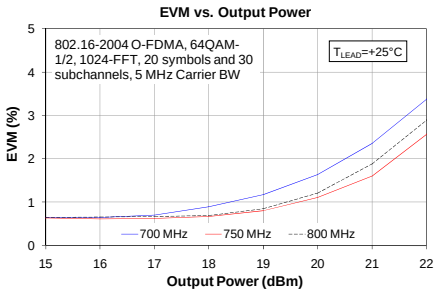
Notes:

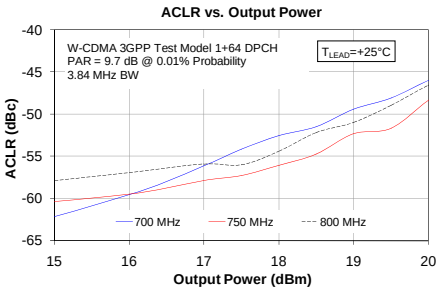
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C11 is placed at 40 mil from AH125 RFout pin. (1.7° @ 750 MHz)
5. The edge of R3 is placed at 210 mil from the edge of C11. (8.7° @ 750 MHz)
6. The edge of C9 is placed next to the edge of R3.
7. The edge of R1 is placed at 100 mil from AH125 RFin pin. (4.2° @ 750 MHz)
8. The edge of C10 is placed 250 mil from the edge of R1. (10.4° @ 750 MHz)











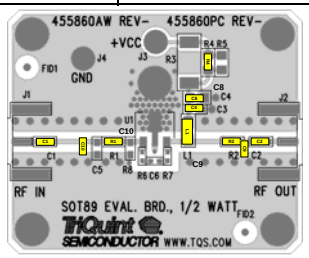
Note: For improved output return loss, ≥10dB, please contact TriQuint applications support for a reference design employing feedback. Corresponding OIP3 performance will be ~+43dBm.

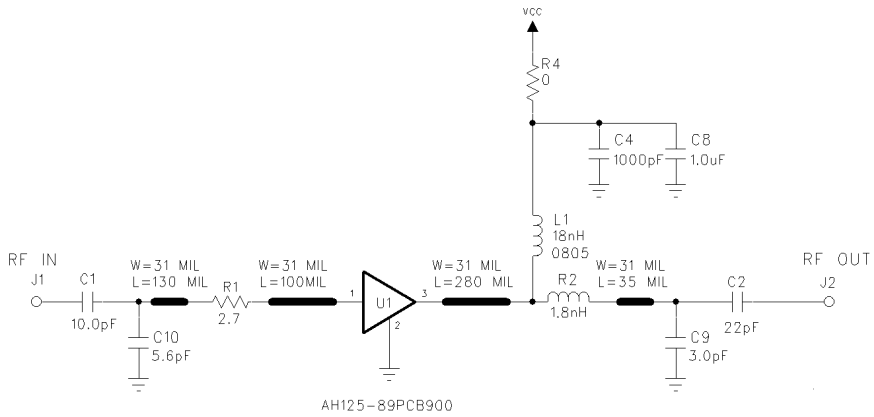
869-960 MHz Reference Design (AH125-89PCB900)

W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW

Typical W-CDMA Performance at 25°C

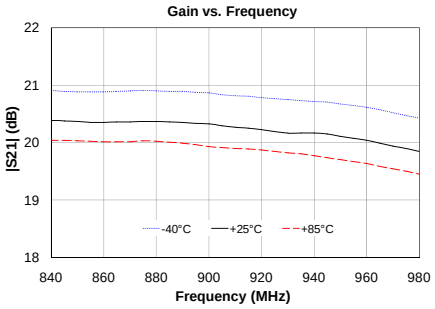
Frequency	869	920	960	MHz
Gain	20	20	20	dB
Input Return Loss	14	20	22	dB
Output Return Loss	10	9.9	9.9	dB
ACLR Pout=+18 dBm	-52	-52.5	-52	dBc
Output P1dB	+27.4	+28.1	+27.9	dBm
Output IP3 Pout=+17dBm/tone, 1MHz spacing	+44	+47	+49	dBm
Noise Figure	7.9	7.7	7.5	dB
Quiescent Current, Icq	150			mA
Vcc	+5			V

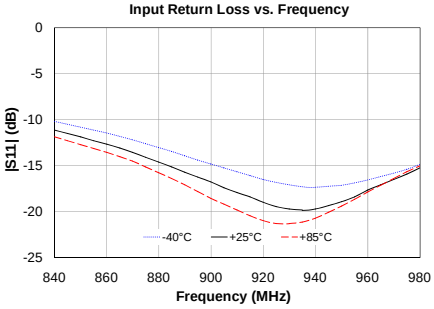


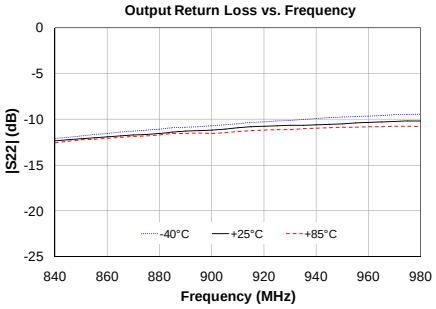


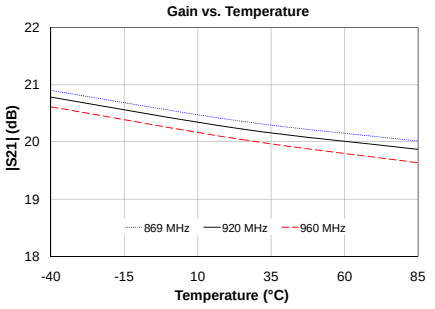
Notes:

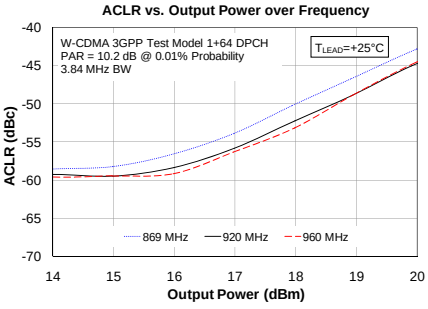
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of R2 is placed at 280 mil from AH125 RFout pin. (14.3° @ 920 MHz)
5. The edge of C9 is placed 35 mil from the edge of R2. (1.8° @ 920 MHz)
6. The edge of R1 is placed at 100 mil from AH125 RFin pin. (5.1° @ 920 MHz)
7. The edge of C10 is placed 130 mil from the edge of R1. (6.6° @ 920 MHz)

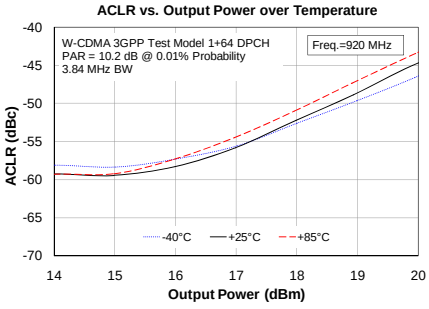


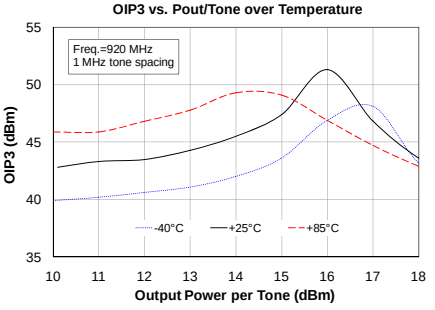


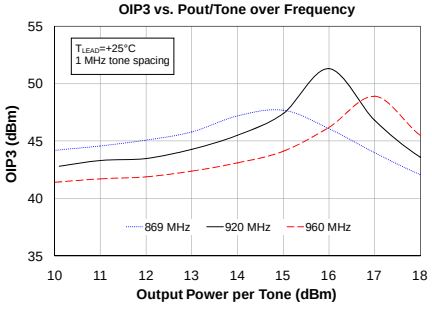


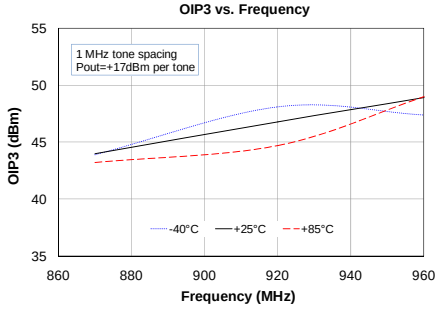






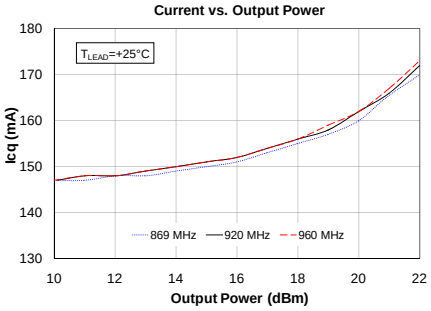


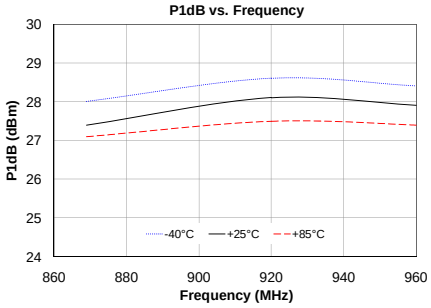


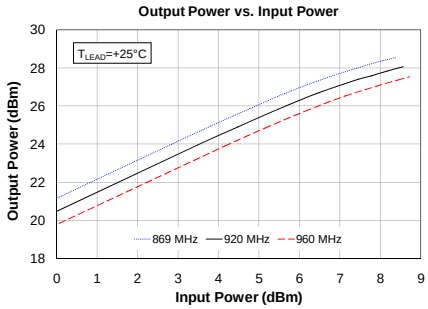


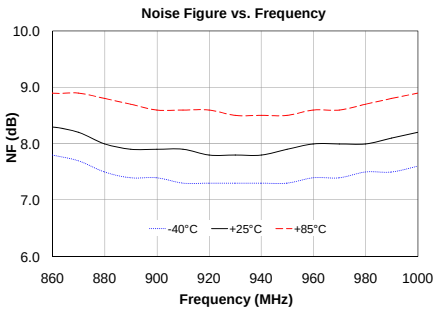
869-960 MHz Reference Design (AH125-89PCB900)

W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW







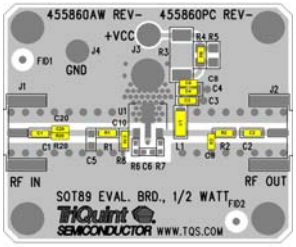


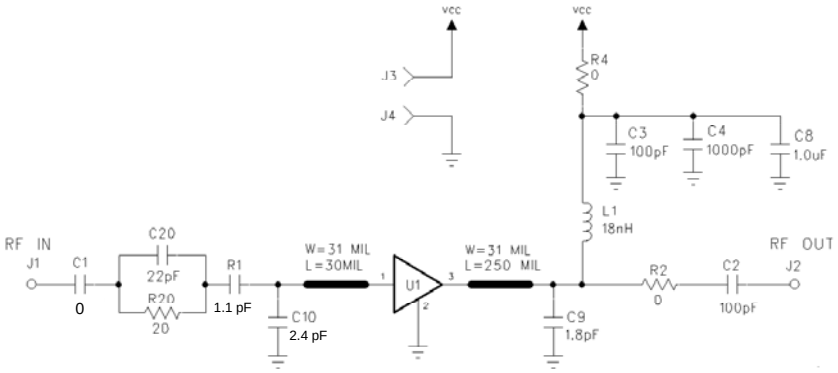
1805-1880 MHz Reference Design

W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW

Typical W-CDMA Performance at 25°C

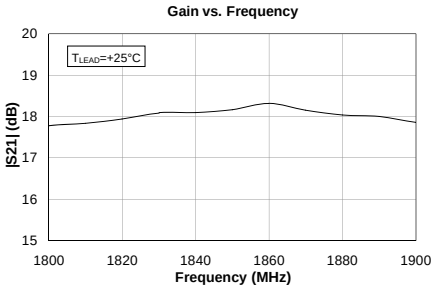
Frequency	1805	1842	1880	MHz
Gain	17.8	18.2	18.1	dB
Input Return Loss	9.5	16.5	17.0	dB
Output Return Loss	9.4	8.4	7.8	dB
ACLR Pout=+18 dBm	-51	-51	-49	dBc
Output P1dB	+28	+27.9	+27.8	dBm
Output IP3 Pout=+14dBm/tone, 1MHz spacing	+44	+45	+43.5	dBm
Quiescent Current, Icq	150			mA
Vcc	+5			V

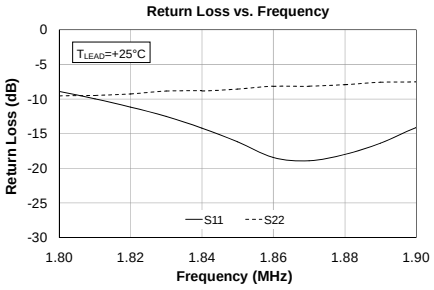


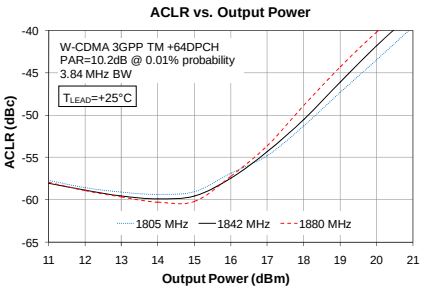


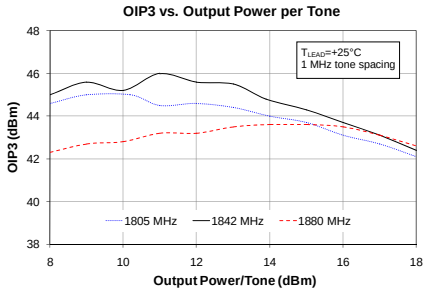
Notes:

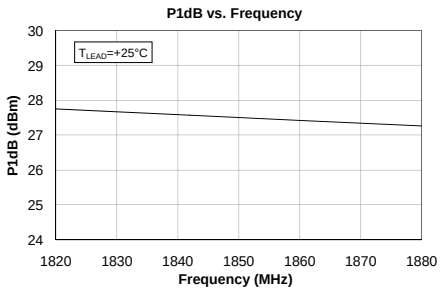
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 250 mil from AH125 RFout pin. (25.5 ° @ 1845 MHz)
5. The edge of R1 is placed against the edge of C10.
6. The edge of C10 is placed at 30 mil from AH125 RFin pin. (3.1 ° @ 1845 MHz)









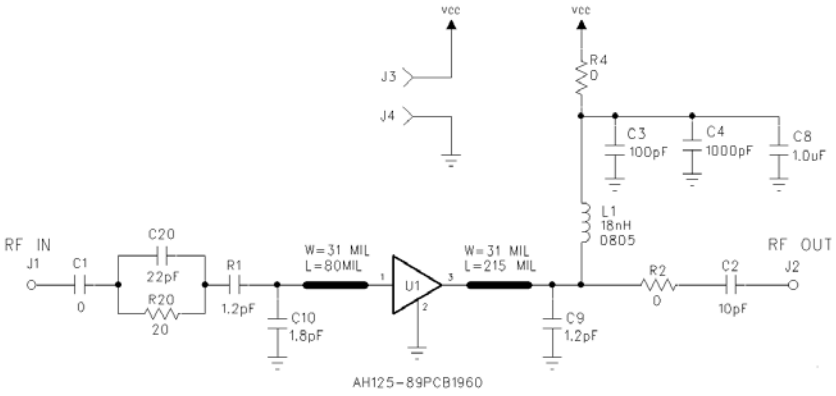


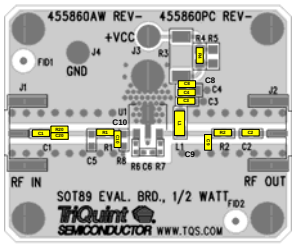
1930-1990 MHz Reference Design (AH125-89PCB1960)

W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW

Typical W-CDMA Performance at 25°C

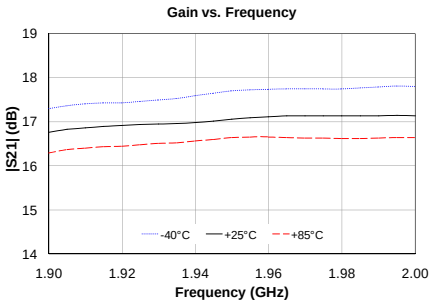
Frequency	1930	1960	1990	MHz
Gain	17	17	17	dB
Input Return Loss	12	16	23	dB
Output Return Loss	10	9	8	dB
ACLR Pout=+18 dBm	-53	-53	-53	dBc
Output P1dB	+27.8	+27.8	+27.7	dBm
Output IP3 Pout=+14dBm/tone, 1MHz spacing	+45	+47	+47	dBm
Noise Figure	4.5	4.6	4.6	dB
Quiescent Current, Icq	150			mA
Vcc	+5			V

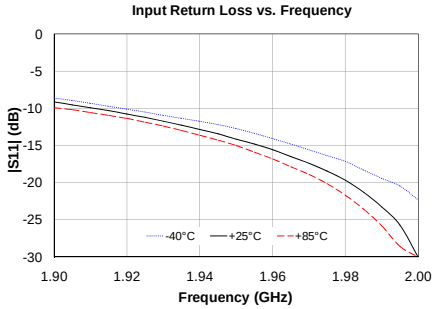


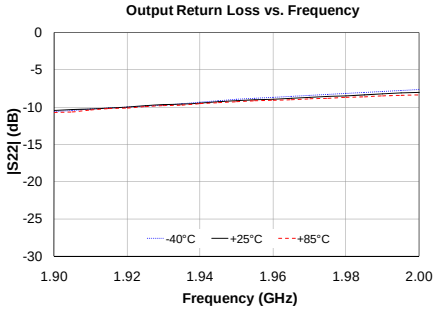


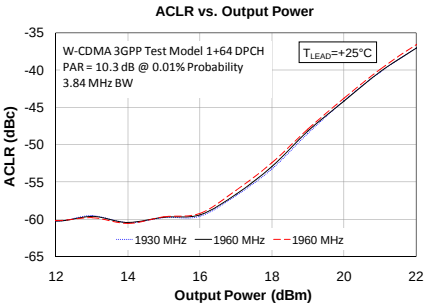
Notes:

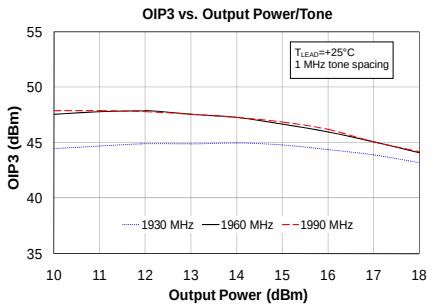
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 215 mil from AH125 RFout pin. (23.3 ° @ 1960 MHz)
5. The edge of R1 is placed against the edge of C10.
6. The edge of C10 is placed at 80 mil from AH125 RFin pin. (8.7 ° @ 1960 MHz)

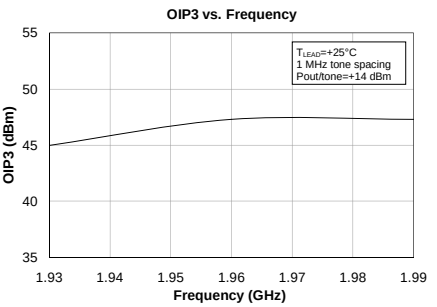


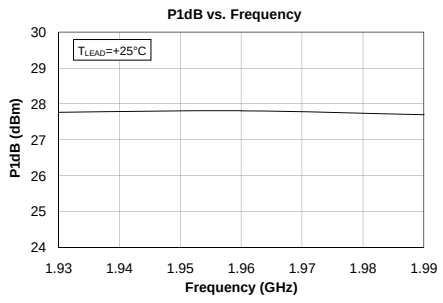


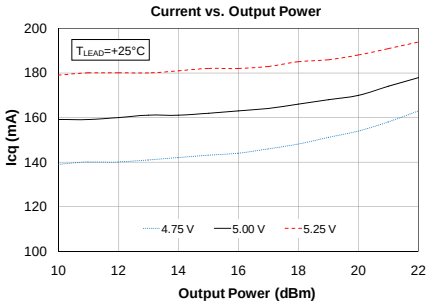


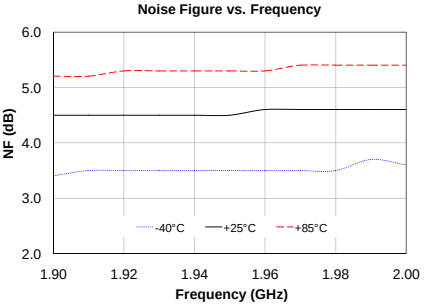










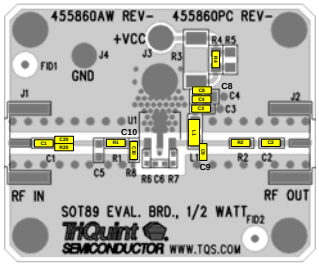


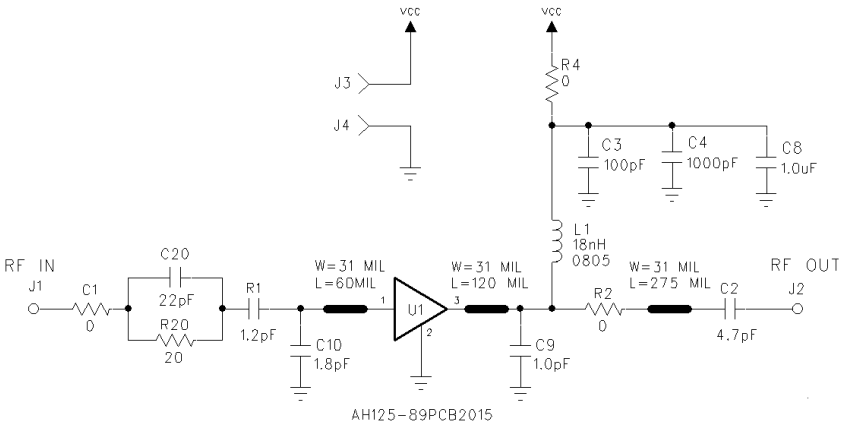
2010-2025 MHz Reference Design

TD-SCDMA 3 Carrier, PAR = 10 dB @ 0.01% Probability, 1.28 MHz BW

Typical TD-SCDMA Performance at 25°C

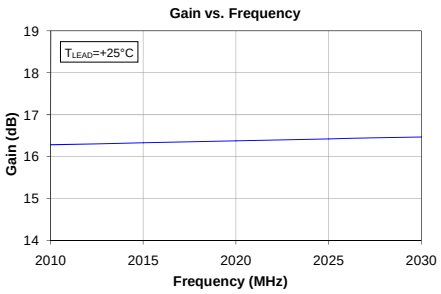
Frequency	2010	2015	2025	MHz
Gain	16.3	16.3	16.4	dB
Input Return Loss	12.6	13.1	14.4	dB
Output Return Loss	8.2	8.1	7.9	dB
ACLR Pout=+16 dBm	-49.5	-50	-50.1	dBc
Output P1dB	+28	+28.3	+28	dBm
Output IP3 Pout=+10 dBm/tone, 1MHz spacing	+45	+45	+45	dBm
Quiescent Current, Icq	150			mA
Vcc	+5			V

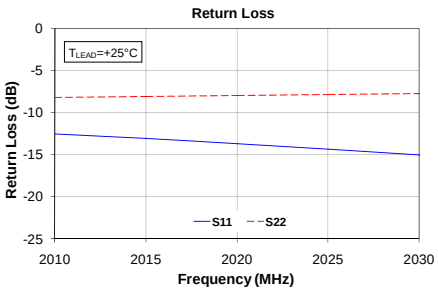


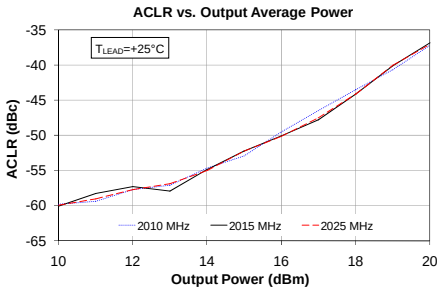


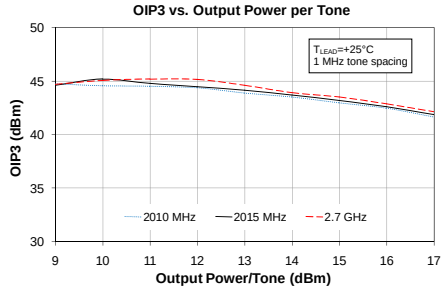
Notes:

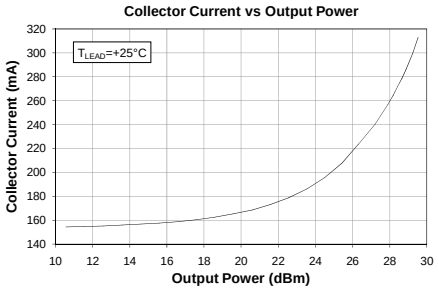
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 120 mil from AH125 RFout pin. (13.4° @ 2015 MHz)
5. The edge of C2 is placed 275 mil from the edge of C9. (30.7° @ 2015 MHz)
6. The edge of C10 is placed at 60 mil from AH125 RFin pin. (6.7° @ 2015 MHz)
7. The edge of R1 is placed next to the edge of C10.

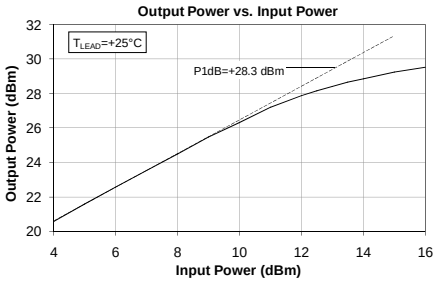










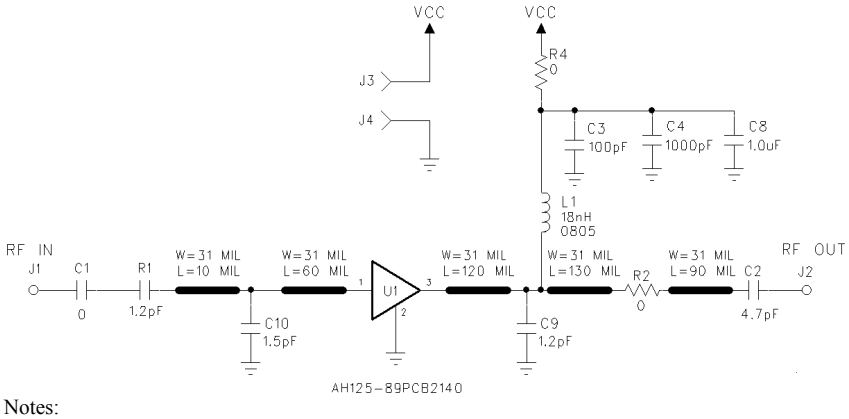


2110-2170 MHz Reference Design (AH125-89PCB2140)

W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW

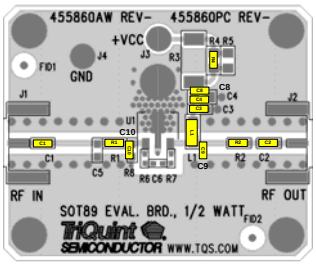
Typical W-CDMA Performance at 25°C

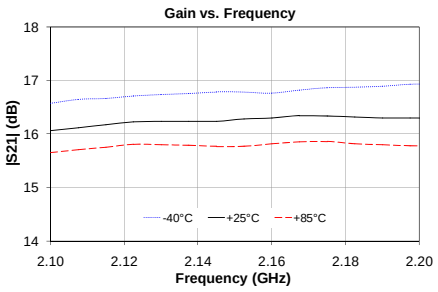
Frequency	2110	2140	2170	MHz
Gain	16.1	16.2	16.3	dB
Input Return Loss	10	12	15	dB
Output Return Loss	13	12	11	dB
ACLR Pout=+18 dBm	-52	-52	-52	dBc
Output P1dB	+28	+28	+28	dBm
Output IP3 Pout=+12 dBm/tone, 1MHz spacing	+49	+45	+47	dBm
Noise Figure	4.3	4.4	4.4	dB
Quiescent Current, Icq	150			mA
Vcc	+5			V

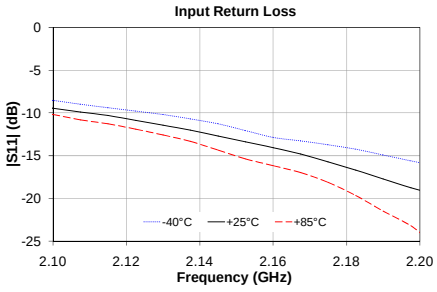


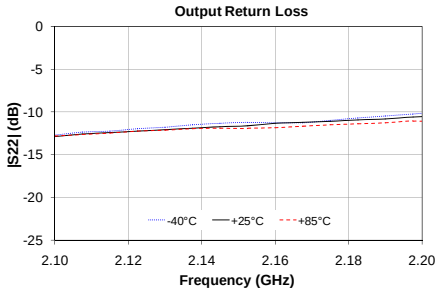
Notes:

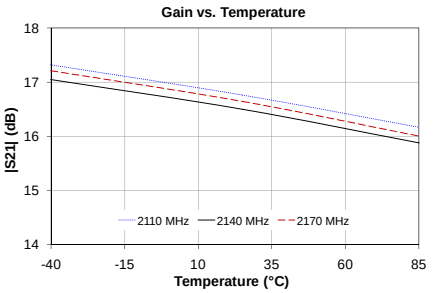
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 120 mils from AH125 RFout pin. (14.2 ° @ 2140 MHz)
5. The edge of C2 is placed at 280 mils from the edge of C9. (33.2 ° @ 2140 MHz)
6. The edge of C10 is placed at 60 mils from AH125 RFin pin. (7.1 ° @ 2140 MHz)
7. The edge of R1 is placed 10 mils from the edge of C10. (1.2 ° @ 2140 MHz)

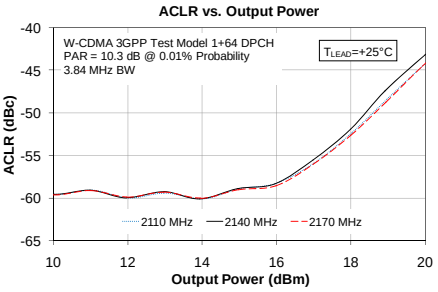


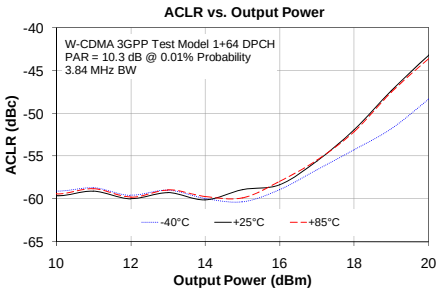


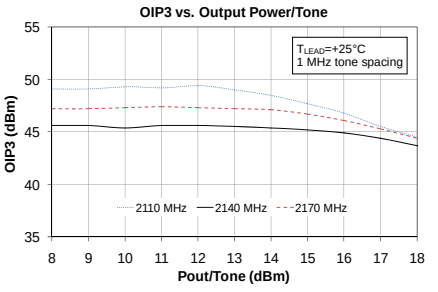


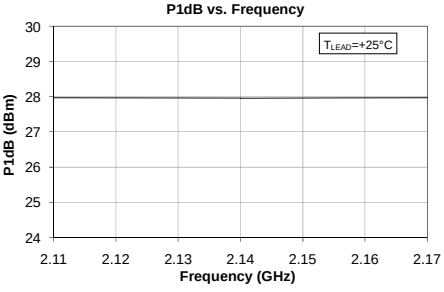


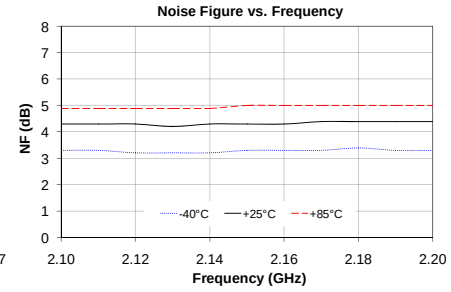










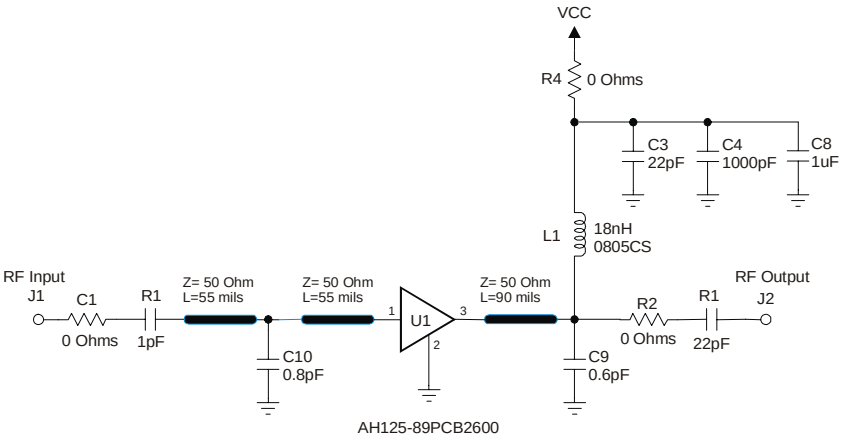


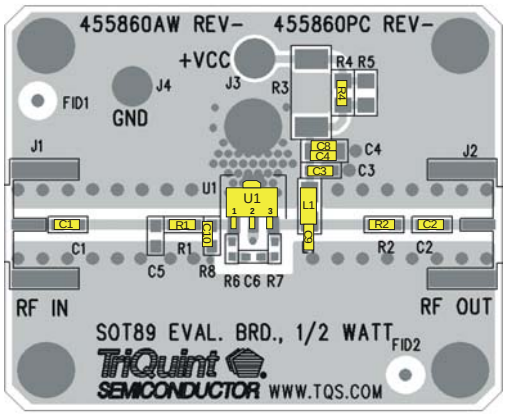
2.5-2.7 GHz Reference Design

802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW

Typical Performance at 25°C

Frequency (GHz)	2.5	2.6	2.7	Units
Gain	13.9	14.0	13.7	dB
Input Return Loss	9.5	13.1	12.9	dB
Output Return Loss	9.4	8.7	8.2	dB
EVM Pout=+19 dBm	1.5	1.25	1.3	%
Output P1dB	+28	+28	+28	dBm
Output IP3 Pout=+16 dBm/tone, 1MHz spacing	+49	+48	+47	dBm
Quiescent Current, Icq	150			mA
Vcc	+5			V

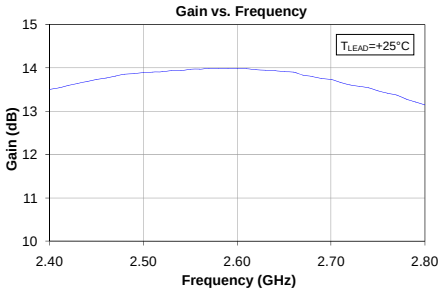


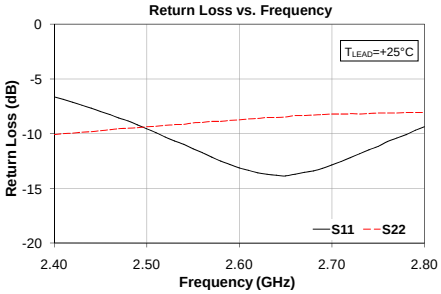


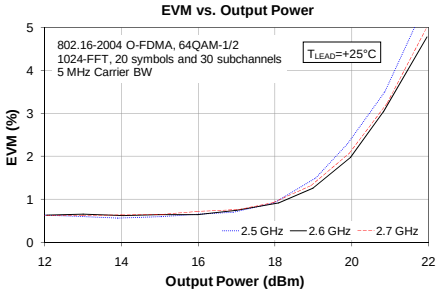
Circuit Board Material: 0.014" FR4, single layer, 1 oz copper, ε_r = 4.3,
Microstrip line details: width = .031", spacing = .035"

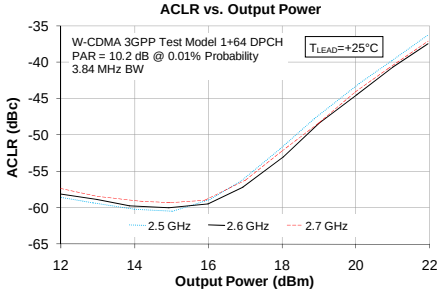
Notes:

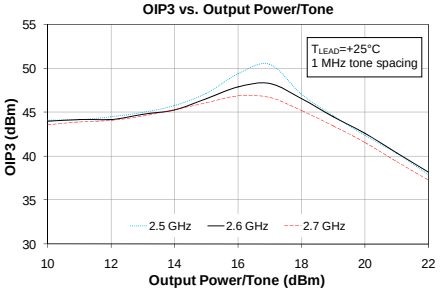
9. The primary RF microstrip line is 50 Ω.
10. Components shown on the silkscreen but not on the schematic are not used.
11. 0 Ω jumpers can be replaced with copper trace in target application.
12. Distance from side edge of C10 to side edge of U1 pin 1 is 55 mils (7.9°@2600 MHz).
13. Distance from end edge of R1 to side edge of U1 pin 1 is 110 mils (15.8°@2600 MHz)..
14. Distance from side edge of C9 to side edge of U1 pin 3 is 90 mils (13.0°@2600 MHz)..









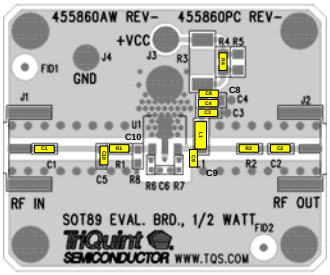


3.4-3.6 GHz Reference Design

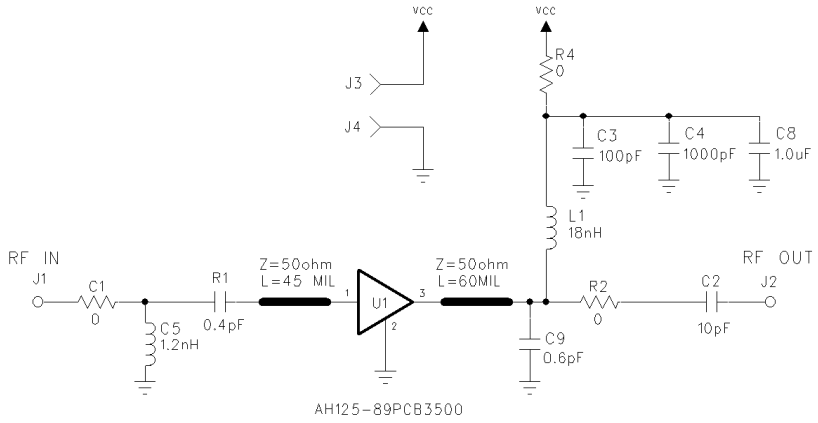
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW

Typical O-FDMA Performance at 25°C

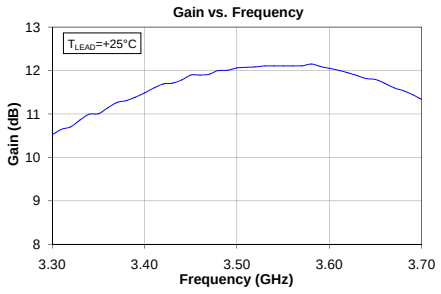
Frequency	3.4	3.5	3.6	GHz
Gain	11.5	12.1	12	dB
Input Return Loss	8	15	21	dB
Output Return Loss	16	13	11	dB
EVM Pout=+18 dBm	1.1	1.0	1.1	%
Output P1dB	+27	+27.3	+27.5	dBm
Output IP3 Pout=+16 dBm/tone, 1MHz spacing	+49.5	+45.7	45.2	dBm
Quiescent Current, Icq	150			mA
Vcc	+5			V

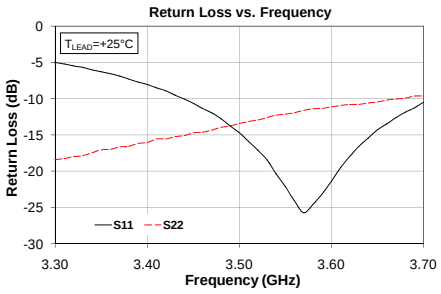


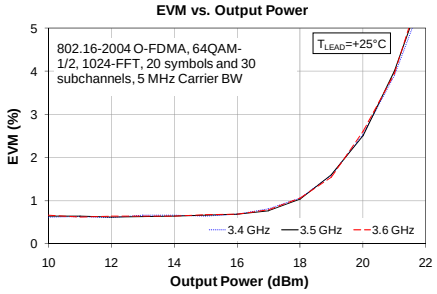
Circuit Board Material: 0.014" FR4, single layer, 1 oz copper, ε_r = 4.3,
Microstrip line details: width = .031", spacing = .035"

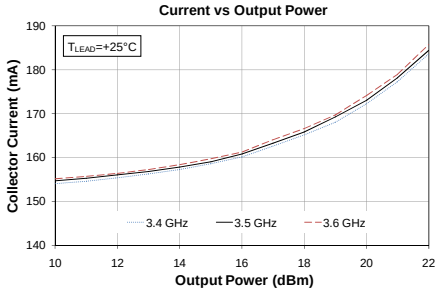


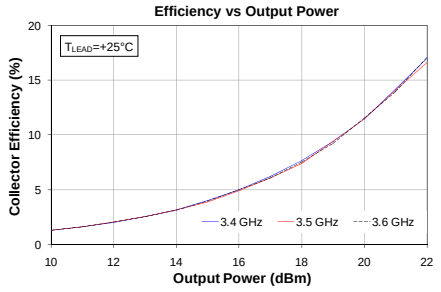
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 60 mil from AH125 RFout pin. (11.6° @ 3.5 GHz)
5. The edge of C10 is placed at 45 mil from AH125 RFin pin. (8.7° @ 3.5 GHz)
6. The edge of L2 is placed next to the edge of C10.

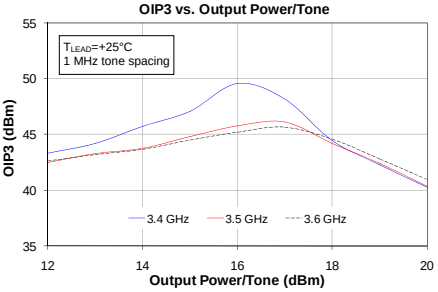










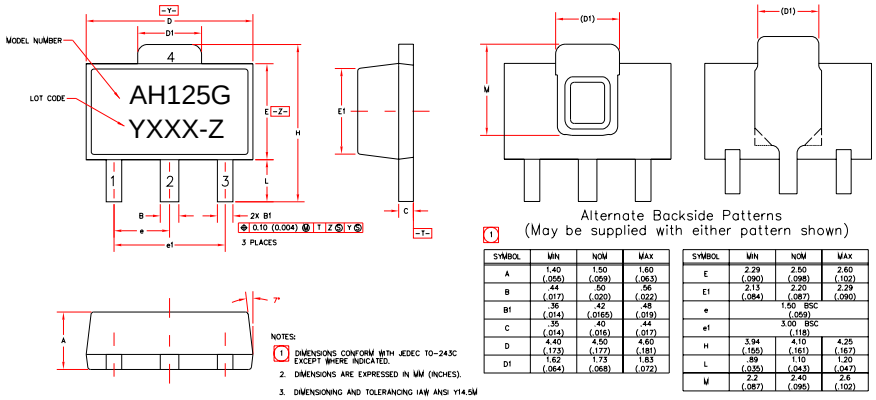


Note: This reference design was constructed on FR4 to illustrate potential AH125 performance in the 3.4-3.6 GHz frequency range. For customer applications of AH125 at these frequencies, we recommend the use of more suitable materials such as Rogers 3000 series.

Mechanical Information

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

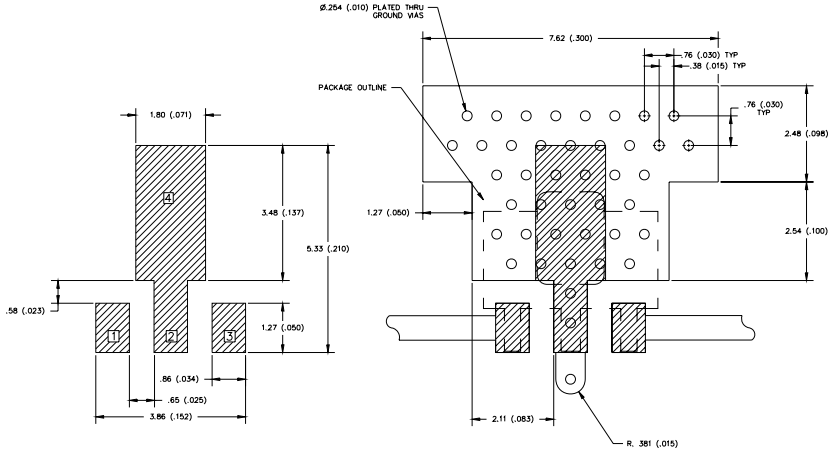
Outline Drawing



SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e	1.50 BSC (.059)		
e1	3.00 BSC (.118)		
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Land Pattern



Product Marking

The AH125 will be marked with an "AH125G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXX" is an auto-generated number, and "Z" refers to a wafer number in a batch.

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating:	Class 2
Value:	Passes ≥2000V to <4000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 2000V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating:	Level 3 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.